4-WAY SUPERSCALAR + VECTOR-REGISTER PROCESSOR DESIGN with Parallel Neuron Transfer Functions

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MAIN DESIGN

The overall design of the project involves a main code stack and dispatch unit as a part of a 4-way processor unit. This means that the processor designed is capable of performing 4 operations at once.
Additionally, the processor is capable of scalar and vector operations, these operations are being determined by the OP code that is specified in the design specifications for the project. The OP code is input into the project and then spread throughout the rest of the project to guide all of the actions taken.

LOGISIM

Logisim comes prebuilt with a subcircuit function. This function allows circuits to be represented by a box with inputs and outputs. This allows for such a complex circuit to visible on a single screen.

DESIGN SPECIFICATIONS

MACHINE INSTRUCTION SET

SCALAR ARITHMETIC ADDITION
- 00h (OP-CODE = 00000000) Ri + counter#1 →Rk
- 01h (OP-CODE = 00000001) Ri + counter#2 →Rk
- 02h (OP-CODE = 00000010) Ri + Rj →Rk
- 03h (OP-CODE = 00000011) counter#1 + counter#2 →Rk

SCALAR ARITHMETIC SUBTRACTION
- 04h to 07h (OP-CODE = 000001XX) *Reserved for future subtraction instructions*

SCALAR ARITHMETIC MULTIPLICATION
- 08h (OP-CODE = 00001000) Ri x counter#1 →Rk, overflow →R(k+1)
- 09h (OP-CODE = 00001001) Ri x counter#2 →Rk, overflow →R(k+1)
- 0Ah (OP-CODE = 00001010) Ri x Rj →Rk, overflow →R(k+1)
- 0Bh (OP-CODE = 00001011) counter#1 x counter#2 →Rk, overflow→R(k+1)

SCALAR ARITHMETIC DIVISION
- 0Ch to 0Fh (OP-CODE = 000011XX) *Reserved for future division instructions*

SCALAR ARITHMETIC COMPARISON
- 10h (OP-CODE = 00010000) Compare Ri with counter#1 →Rk
- 11h (OP-CODE = 00010001) Compare Ri with counter#2 →Rk
- 12h (OP-CODE = 00010010) Compare Ri with Rj →Rk
- 13h (OP-CODE = 00010011) Compare Counters

SCALAR LOGICAL AND
- 20h (OP-CODE = 00100000) Ri AND counter#1 →Rk
- 21h (OP-CODE = 00100001) Ri AND counter#2 →Rk
- 22h (OP-CODE = 00100010) Ri AND Rj →Rk
- 23h (OP-CODE = 00100011) AND counters →Rk

SCALAR LOGICAL OR
- 24h (OP-CODE = 00100100) Ri OR counter#1 →Rk
- 25h (OP-CODE = 00100101) Ri OR counter#2 →Rk
- 26h (OP-CODE = 00100110) Ri OR Rj →Rk
- 27h (OP-CODE = 00100111) OR counters →Rk

CLEAR
- 30h (OP-CODE = 00110000) Clear Ri

VECTOR/ARRAY / MATRIX and NEURON INSTRUCTIONS
Vi, Vj, and Vk are created from outputs of the four parallel scalar functional units

VECTOR ARITHMETIC ADDITION
- 82h (OP-CODE = 10000010) Vi + Vj →Vk

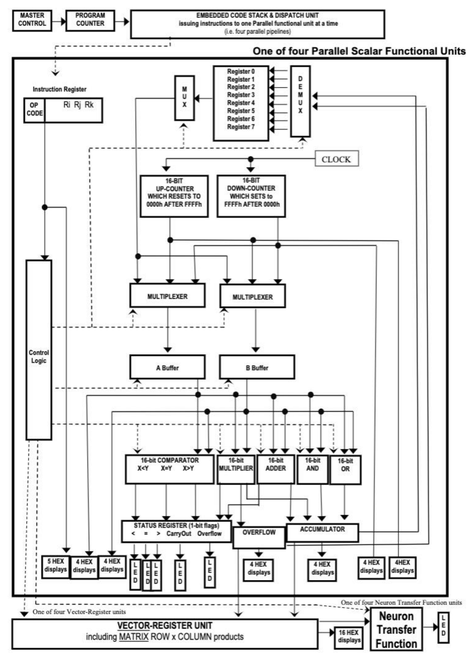
VECTOR ARITHMETIC SUBTRACTION
- 84h to 87h (OP-CODE = 100001XX) *Reserved for future subtraction instructions*

VECTOR ARITHMETIC MULTIPLICATION
- 0Ah (OP-CODE = 10001010) Vi x Vj →Vk, overflow →V(k+1)

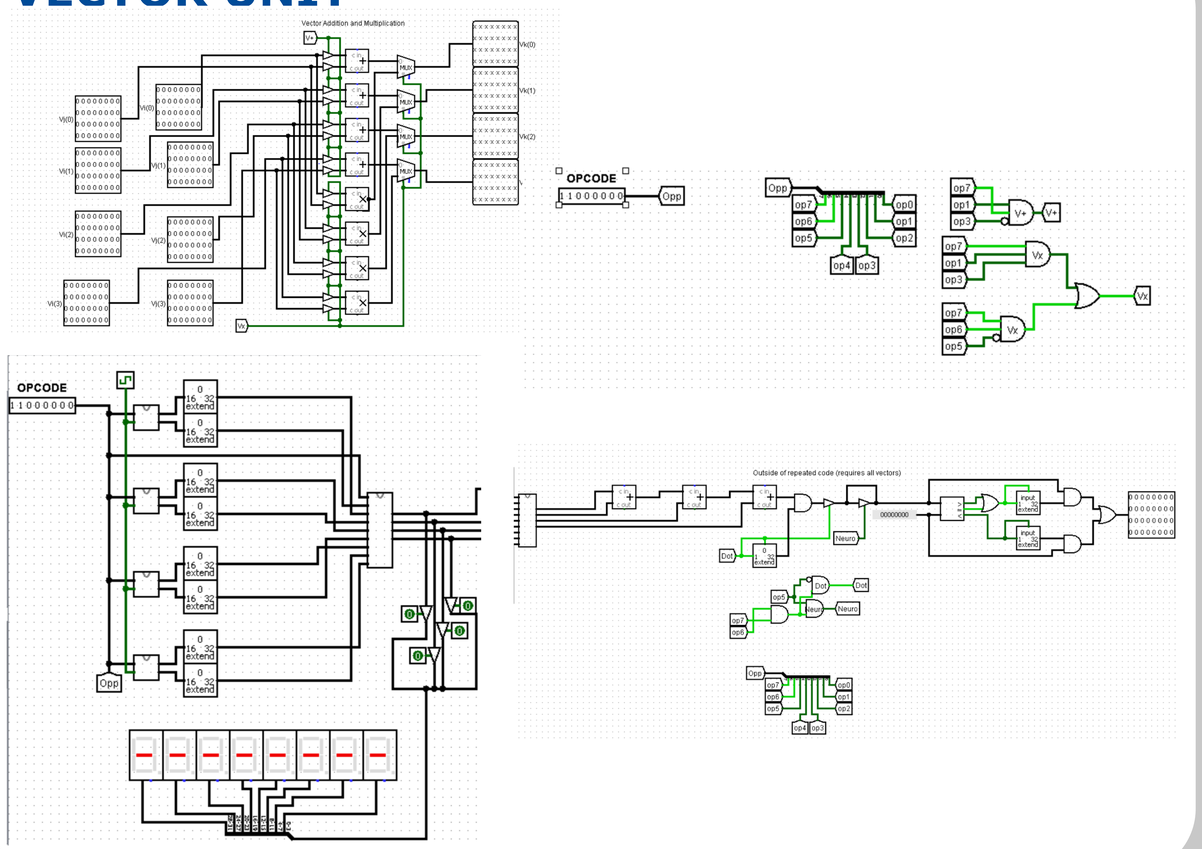
VECTOR ARITHMETIC DIVISION
- 8Ch to 8Fh (OP-CODE = 100011XX) *Reserved for future division instructions*

MATRIX ROW x COLUMN (i.e., Dot-Product)
- C0h (OP-CODE = 11000000) Vi x Vj →Vk, overflow →V(k+1)
  Vk(1)+Vk(2)+Vk(3)+Vk(4) → 32-Bit Scalar Accumulator

NEURON TRANSFER FUNCTION
- E0h (OP-CODE = 11100000) Vi x Vj →Vk, overflow →V(k+1)
  Vk(1)+Vk(2)+Vk(3)+Vk(4) → 32-Bit Scalar Accumulator
  32-Bit Scalar Accumulator → **Neuron Transfer Function**



VECTOR UNIT



SCALAR UNIT